SoC-powered Linux

Benefits of Linux-powered SoC-devices





Presentation plan

- Company profile
- SoC Altera Cyclone V Architecture
- Booting Linux: SPL, U-boot, kernel
- Developing NIC
- Benchmarks
- Troubles



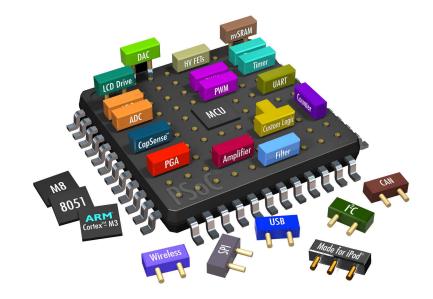
STC Metrotek

- 12 years of RnD experience
- Russia, Saint-Petersburg
- Development and production of measurement equipment
- Telecommunication channels verification: E1, Datacom, Ethernet (10/100/GbE/10G/100G), fiber optics
- Network packet analysis and processing at line rate
- From idea to complete to "out of the box" solution
- Linux inside!

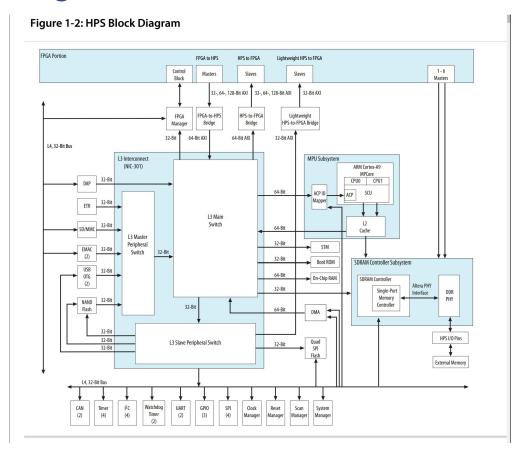


System On Chip

one chip integrates many components

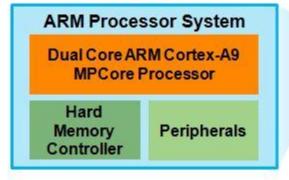


SoC block diagram



Altera SoC = HPS(CPU) + FPGA





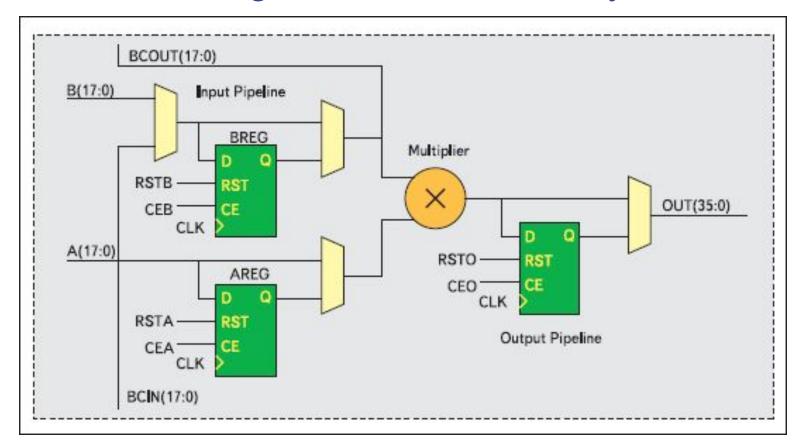


28-nm FPGA



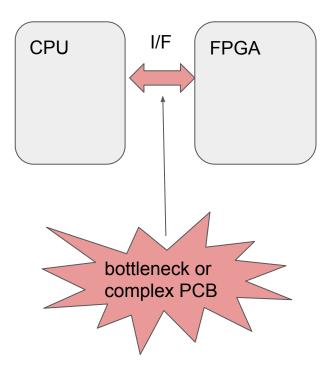


FPGA - Field Programmable Gate Array

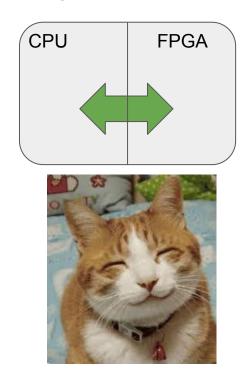


Why use SoC?

Old school

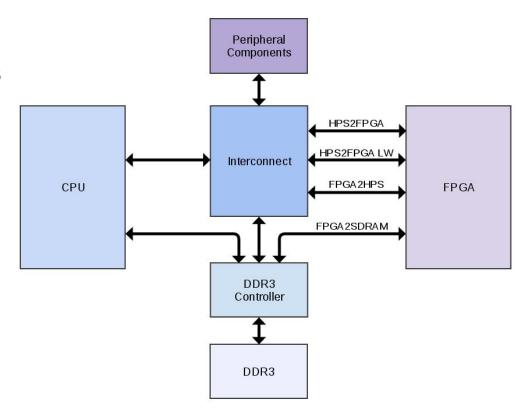


Modern design

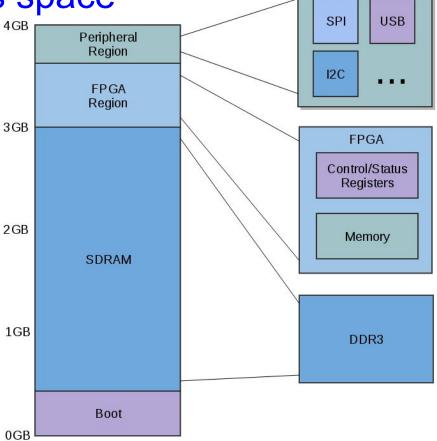


SoC data flows

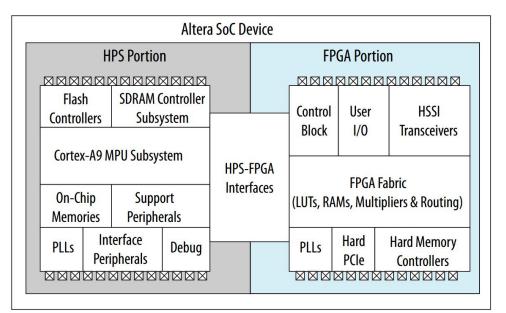
- Direct memory access
- Interconnect
- Dedicated HPS-FPGA interfaces



CPU address space

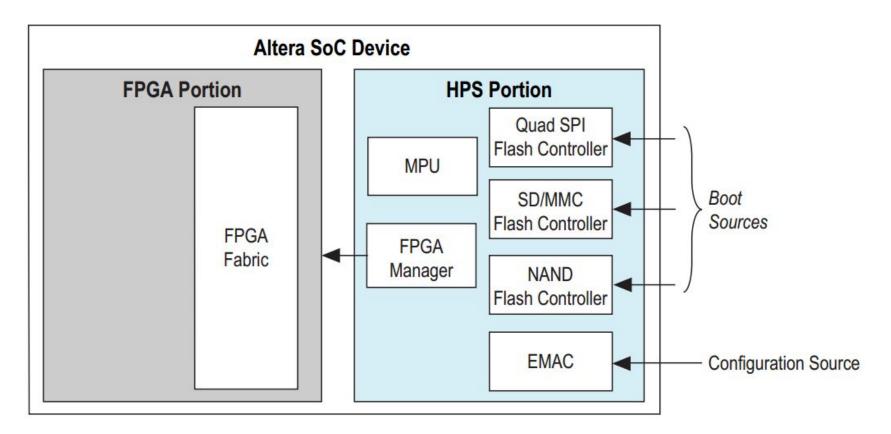


SoC architecture

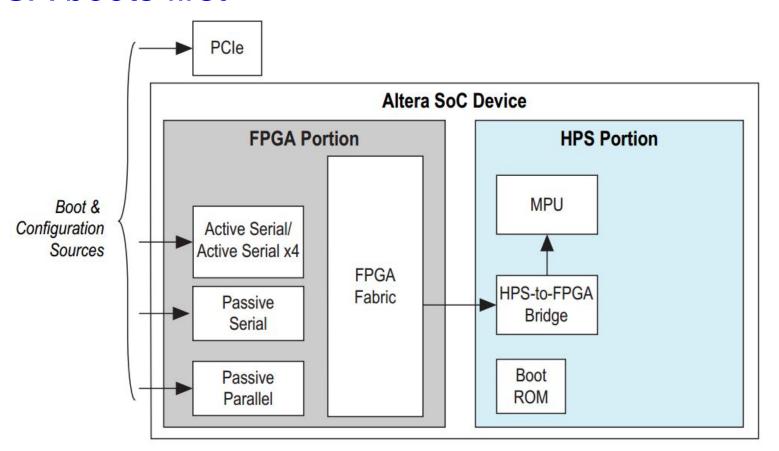


- Independent HPS and FPGA
- Boot sources: SD, QSPI, etc...
- Independent flexible configuration (HPS or FPGA initiated)
- Dedicated memory for FPGA registers
- High-speed interfaces

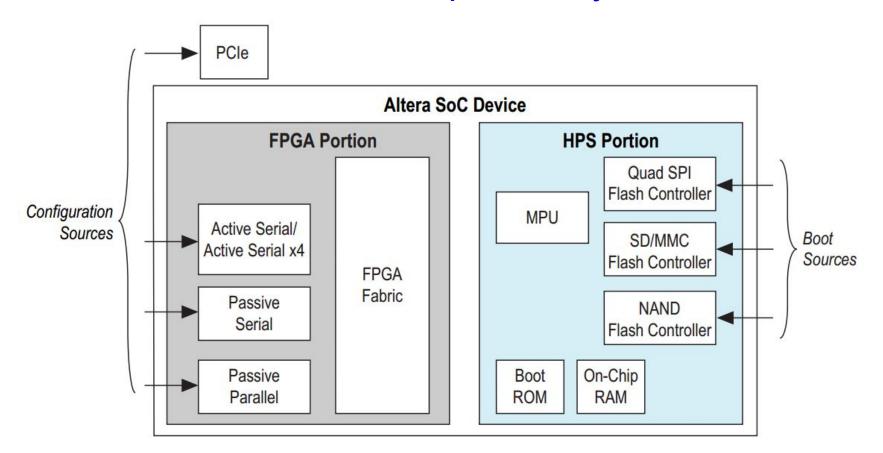
CPU boots first



FPGA boots first

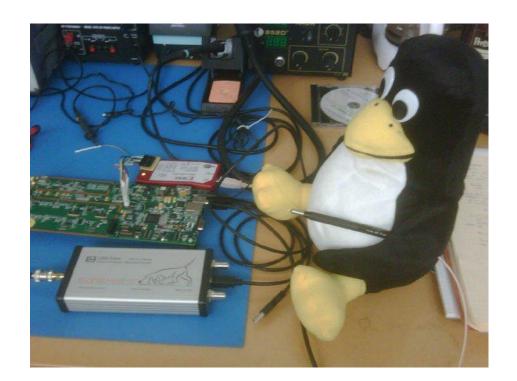


HPS and FPGA boots independently

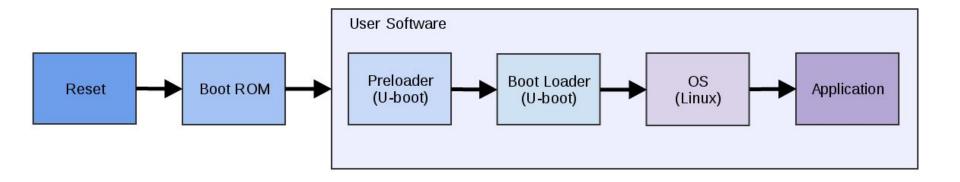


Booting Linux

- preloader
- U-boot + environment
- device tree
- Linux kernel
- rootfs



HPS Boot flow



Preloader + U-boot

Preloader

- DDR initialization
- memtest
- basic synchronization clock setup



U-boot

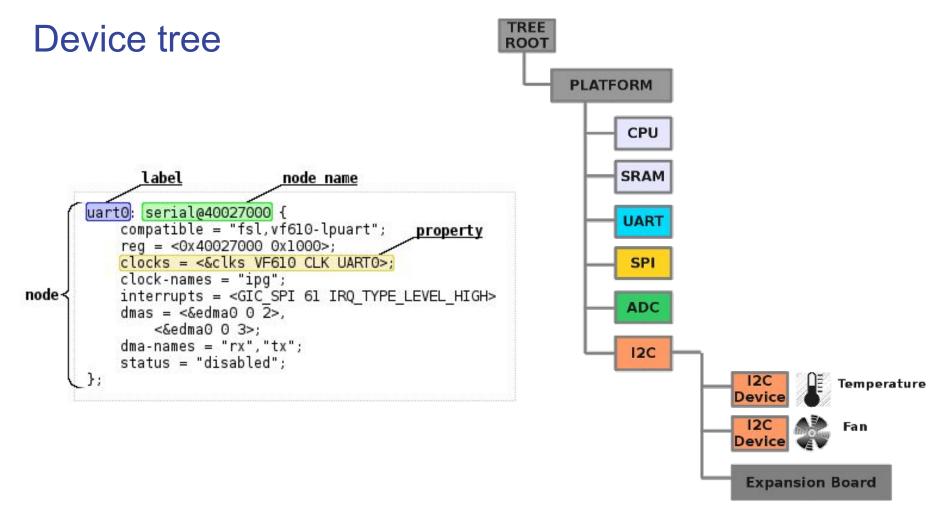
- access to peripheral (SD/USB/Ethernet/i2c/etc..)
- filesystem support (fat/ext2)
- flexible boot configuration (boot from TFTP, RAM, etc...)
- scripting, flexibility
- direct memory access



Linux kernel

- github:altera-opensource/linux-socfpga
- v 3.18.0





Booting FPGA

- Load fpga manager module
- Ensure that FPGA has been detected -- file /dev/fpga0 should exist
- Get proper FPGA firmware file -- firmware.rbf
- Load it to FPGA -- cat firmware.rbf > /dev/fpga0
- Ensure that it has been loaded -- cat /sys/class/fpga/fpga0/status

HPS and FPGA ready for data exchange!

Moving to practical examples



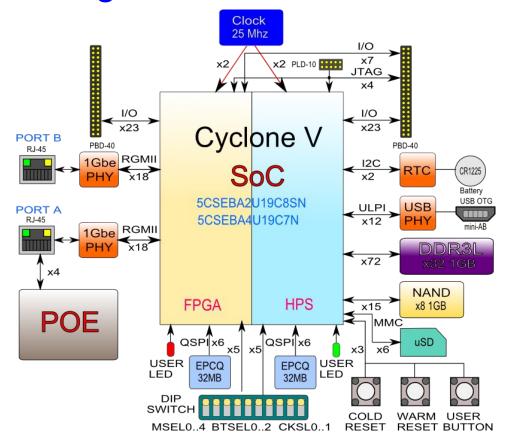
EthOnd development board

Features:

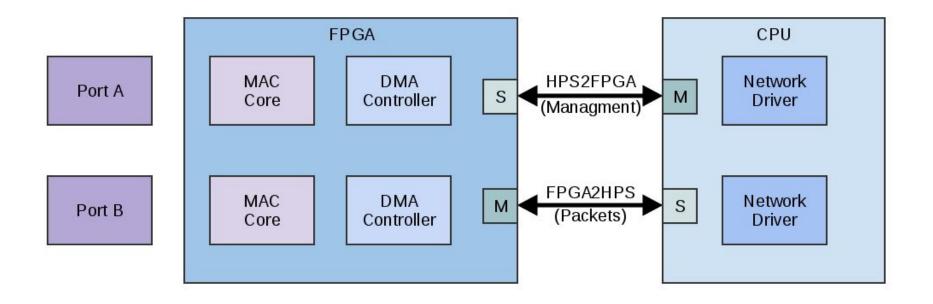
- SoC with 2 ARMv7 Cores and FPGA
- RAM 1GB
- SD-card slot
- 2 x GbE ports
- Shield interface
- USB OTG
- UART console
- Optional PoE
- RTC



EthOnd block diagram



NIC block diagram

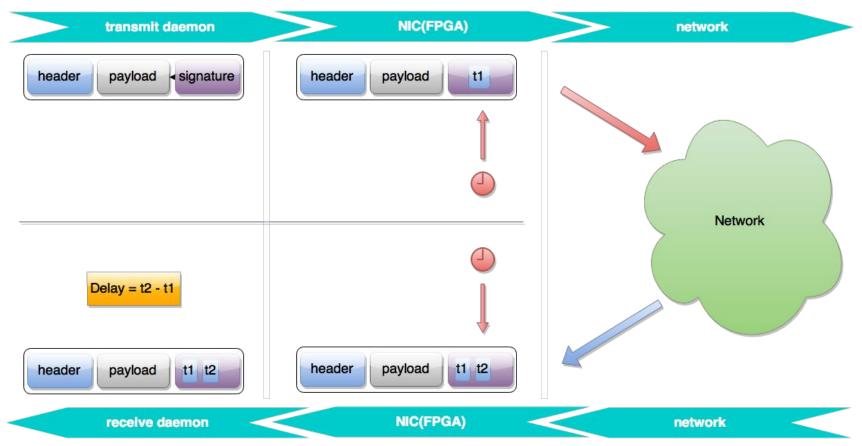


NIC Features

- 2 ports
- NAPI support
- frame sizes 64-1518
- DMA support
- 10/100/1000 Mbps, full duplex
- ethtool support (link speed, link status)
- MDIO support
- low-level timestamping



Packet timestamping



NIC Benchmarks

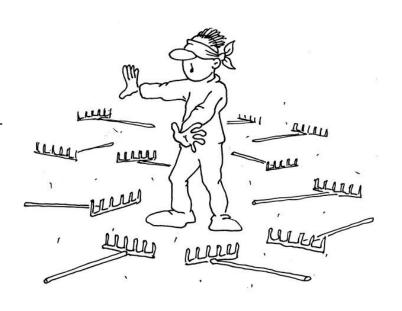
- TCP iperf on 1500 bytes, TCP window size 85K -- 370 Mbit/s
- UDP for different frame sizes: 16 377 Mbit/s
- Delay via office switch 3 us



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Troubles...

- Hardware MAC (stmmac) did not communicate with FPGA
- Sometimes Qsys generates invalid interconnect
- DDR3: 66 MHz instead of 333 MHz
- i2c controller hangs up
- Linux v3.18 has issue with i2c interrupts
- U-boot does not support ULPI
- Linux 3.12 hangs up with pre-loaded FPGA
- fpga2sdram interface should be configured in Uboot
- UART generates thousands of interrupts in 3.18



Pros and cons

- Single chip
- High-speed interconnect
- Linux kernel
- Flexibility

- CPU frequency cannot be changed at run-time
- High chip temperature
- Drivers are still crude yet;)

Thank you!